Remarks

The above Amendments and these Remarks are in reply to the Office action mailed May 13, 2005. Currently, claims 1-44 are pending. Applicants have amended claims 1, 9, 20, 24, 35, and 42. Applicants respectfully request reconsideration of claims 1-44.

I.   Rejection of Claims 1, 4, 8, 15, 18, and 21 under 35 U.S.C. § 102(e)

Claims 1, 4, 8, 15, 18 and 21 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,438,595 (the '595 patent). Because the '595 patent fails to disclose each limitation of claims 1, 4, 8, 15, 18, and 21 pending after entry of the present amendments, Applicants assert that these claims are patentable over the cited art.

Claims 1, 4, and 8

After amendment, claim 1 recites:

> A switch for use in a network, comprising:
> a plurality of linecards, each including:
>   a plurality of ports; and
>   a plurality of <u>storage protocol</u> processing units, wherein each
> storage protocol processing unit is associated with at least one port
> and <u>performs storage command processing</u> for commands received at
> said at least one port, thereby distributing processing resources
> amongst linecard ports. *Emphasis added.*

Amended claim 1 now recites that the processing unit of each linecard is a "storage protocol processing unit" that "performs storage command processing." Because each processing unit is a storage protocol processing unit that performs storage command processing, a storage switch in accordance with claim 1 can perform "various switch-based storage operations, including classification of packets, virtualization, and translation." *See Applicants' Specification ¶ 0100.* The '595 patent does not disclose linecards that include <u>storage protocol</u> processing units that perform <u>storage command processing</u>.

The '595 patent is drawn to the use of "directory services in a data processing system" and as such, teaches that "a directory service of the network is programmed to present a respective view of the network to each host." *The '595 patent, title, abstract.* The described system in the '595 patent includes port adaptors that have "one or more processors for handling the communication protocol of

the data network 21 and communicating with the cache memory busses 33, 34," and storage adaptors that have "one or more processors for handling the communication protocol of the storage devices and for communicating with the cache memory busses 33, 34." *The '595 patent, col. 5, ll. 17-23.* These processors are not "storage protocol processing units" as recited in claim 1. Moreover, they do not perform "storage command processing," as recited in claim 1. For example, a port adaptor in the '595 patent receives storage access requests from hosts and accesses "a directory in the cache memory 32 to determine whether or not the data to be accessed resides in the cache memory." *Id. at col. 4, ll. 37-54.* If it does, the adaptor accesses the data in the cache memory. *See id.* If not, the adaptor forwards "a storage access request to the storage adaptors." *Id.* A storage adaptor responds to the request by determining "where the data to be accessed resides on the storage devices, and reads the data to the cache memory, for access by the port adaptor." *Id.* There is no disclosure in the '595 patent that the processors of the storage adaptors or port adaptors are "storage protocol processing units" that "perform storage command processing," as recited in claim 1.

Because the '595 patent fails to disclose each limitation of claim 1, Applicants respectfully submit that claim 1 is patentable over the cited art. Claims 4 and 8 each ultimately depend from claim 1 and therefore, should be patentable for at least the same reasons.

Claims 15 and 18

Claim 15 recites:

A switch for use in a network, comprising:
a plurality of linecards, each linecard including:
a plurality of ports;
a plurality of processing units, wherein each processing unit is associated with at least one port and is associated with a memory;
a CPU in communication with the processing units; and
<u>a fabric in communication with each linecard, thereby allowing packets to pass from an ingress linecard to an egress linecard.</u>
Emphasis added

Claim 15 recites a storage switch that includes "a fabric in communication with each linecard, thereby allowing packets to pass from an ingress linecard to an egress linecard." A fabric

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enables high speed processing scalable to a number of ports. *See e.g., Applicants' Specification,* ¶ *0070, 0086.* The system disclosed in the '595 patent does not include a fabric "in communication with each linecard."

The '595 patent teaches that the various port and storage adaptors communicate "with the cache memory buses 33, 34" which are connected to "cache memory 32." *The '595 patent, col. 5, ll. 17-23.* A cache memory bus is not a "fabric," as recited in claim 15. While a fabric facilitates high-speed processing, a cache memory and bus entails buffering which slows down processing. Thus, because the '595 patent teaches the communication of its port and storage adaptors through cache memory buses 33, 34, it fails to disclose "a fabric in communication with each linecard, thereby allowing packets to pass from an ingress linecard to an egress linecard," as recited in claim 15.

Because the '595 patent fails to disclose each limitation of claim 15, Applicants respectfully submit that claim 15 is patentable over the cited art. Claim 18 ultimately depends from claim 15 and therefore, should be patentable for at least the same reasons.

Claim 21

Claim 21 recites:

> A switch for use in a system for storing and accessing data, the switch comprising:
> a plurality of linecards, each linecard including:
> at least one port, and
> means associated with each port for performing <u>wire speed processing of packets</u>. *Emphasis added.*

Claim 21 recites that the linecards of the switch include "means associated with each port for performing <u>wire speed processing of packets</u>." *Emphasis added.* Applicants describe that processing data packets at "wire speed" facilitates processing "without introducing any more latency that would be introduced by a switch that merely performed switching or routing functions." *See Applicants' Specification,* ¶ *0015.* It is further described that typically to process data at wire speed, "a storage switch in accordance with an embodiment of the invention will <u>not buffer packets</u>, unlike that done conventionally." *Id (emphasis added).* Thus, wire speed for a switch can be "measured by the connection to the particular port." *Id. at* ¶ *0062.*

The '595 patent describes nothing in the cited portions or elsewhere to support a disclosure or suggestion of "wire speed" processing as recited in claim 21. Nothing within the '595 patent describes how or what techniques could or should be used to accomplish this in a switch. In fact, the figures and text of the '595 patent cited by the Examiner show a cache memory 32 which in a preferred construction is "composed of dynamic RAM memory cards." *The '595 patent, col. 5, ll. 13-15; see Figure 1.* The use of a RAM cache memory is an indication that wire speed processing is not performed. Rather, it is an indication that packets are buffered as described above. *See the '595 patent at col. 4, ll. 37-51.* Thus, the '595 patent does not disclose "means associated with each port for performing wire speed processing of packets," as recited in claim 21.

Because the '595 patent fails to disclose each limitation of claim 21, Applicants assert that claim 21 is patentable over the cited art.

II.   Rejection of Claims 20, 35, and 40-42 under 35 U.S.C. § 102(e)

Claims 20, 35, and 40-42 were rejected under 35 U.S.C. 102 (e) as being anticipated by U.S. Pub. No. 2002/0004883 (the '883 publication). Because the '883 publication fails to disclose each limitation of claims 20, 35, and 40-42, Applicants assert that these claims are patentable over the cited art.

Claim 20

Amended claim 20 recites:

> A switch for use in a system for storing and accessing data, the switch comprising:
> a plurality of linecards, each linecard including:
> at least one port and a plurality of processing units,
> wherein each processing unit is associated with at least one port, and <u>each processing unit includes a classifier, a virtualizer, and a translator</u>;
> <u>a first CPU in communication with each processing unit</u>;   and
> a fabric in communication with each linecard. *Emphasis added.*

Claim 20 recites a switch that includes a plurality of linecards that each include a plurality of processing units and "<u>a first CPU</u> in communication with <u>each</u> processing unit." *Emphasis added.*

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Such a structure as recited in claim 20 aids in wire speed processing. As Applicants teach, data traffic can be "routed to the PPU for wire-speed virtualization and translation, while control traffic such as connection requests or storage management requests are routed to the CPU." *Applicants' Specification,* ¶ *0013.* "Accordingly, unlike the existing art, which forwards all packets to the CPU for processing, a system in accordance with the invention recognizes the packet contents, so that data traffic can be processed separately and faster, aiding in enabling wire-speed processing." *Id.*

The '883 publication does not disclose a switch that includes "a first CPU in communication with each processing unit." It is unclear in the Examiner's general citation to the '883 publication which components therein are asserted to be "processing units" and which is asserted to be the CPU. Applicants can best guess that the Examiner is regarding the "connection blocks CB1-CB9" as the processing units since the '883 publication teaches that these blocks "are where the translation from the physical devices to the desired virtual devices occurs." *The '883 publication,* ¶ *0027.* If this is the case, there clearly is no "CPU in communication with each processing unit," as claim 20 recites. Each connection block is in communication with its own individual CPU or data processor. Referring to Figure 4, CB1 is in communication with data processor DP1, CB2 is in communication with data processor DP2, and so on. There is no single CPU or data processor in communication with "each processing unit" as claim 20 recites. Moreover, if the Examiner is regarding the data processors DP1-DP4 as the "plurality of processing units," it likewise stands that each of these is in communication with an individual connection block. Thus, the '883 publication fails to disclose "<u>a</u> <u>first CPU</u> in communication with <u>each</u> processing unit," as claim 20 recites. *Emphasis added.*

The '883 publication also fails to disclose that "<u>each processing unit includes a classifier, a</u> <u>virtualizer, and a translator</u>." *Emphasis added.* In the '883 publication, the connection blocks CB1-CB9 are "where the <u>translation</u> from the physical devices to the desired virtual devices occurs," while the "NSM (located in the ACSC controller) <u>construct a virtual</u> device with the required data rate." *The '883 publication,* ¶ *0027.* Thus, virtualization and translation in the '883 publication are each performed by discrete devices. Accordingly, the '883 publication does not disclose that "each processing unit includes a classifier, a virtualizer, and a translator," as recited in claim 20.

Because the '883 publication fails to disclose each limitation of claim 20, Applicants assert that claim 20 is patentable over the cited art.

<u>Claim 35, 40, 41</u>

> A storage network, comprising:
> a switch;
> a server in communication with the switch, the server operating in accordance with a first protocol;
> a storage device in communication with the switch, the storage device operating in accordance with a second protocol;
> the switch having an input for receiving data for a virtual target formatted in accordance with the first protocol; and
> the switch having an output for sending the data to a physical target formatted in accordance with the second protocol <u>at wire speed</u>.
> *Emphasis added.*

Claim 35 recites that the switch has an "output for sending the data to a physical target formatted in accordance with the second protocol <u>at wire speed</u>." *Emphasis added.* The '883 publication does not disclose "sending the data to a physical target formatted in accordance with the second protocol <u>at wire speed</u>." In the '883 publication, data is buffered before being transferred to a physical target. The '883 publication teaches that the "data processor DP1 starts transferring data to the Connection Block CB1, which will buffer the data and transfer it to the physical tape devices TD1, TD2, TD3 via CB5, CB6, CB7." *The '883 publication, ¶ 0029.* Because the '883 publication teaches buffering of data before transfer to physical tape devices, it does not disclose "sending the data to a physical target formatted in accordance with the second protocol <u>at wire speed</u>," as recited in claim 35.

Because the '883 publication fails to disclose each limitation of claim 35, Applicants assert that claim 35 is patentable over the cited art. Claims 40 and 41 each ultimately depend from claim 35 and therefore, should be patentable for at least the same reasons.

<u>Claim 42</u>

Similar to claim 35, claim 42 recites "sending the packet to a physical target formatted in accordance with a second protocol <u>at wire speed</u> if said packet is a data packet." *Emphasis added.* As shown with respect to claim 35, the '883 publication fails to disclose sending data packets at wire speed. In the '883 publication, "the connection block will "buffer the data and transfer it to the physical tape devices." *The '883 publication, ¶ 0029.* Thus, the '883 publication fails to disclose

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"sending the packet to a physical target formatted in accordance with a second protocol at wire speed if said packet is a data packet," as recited in claim 42.

Because the '883 publication fails to disclose each limitation of claim 42, Applicants assert that claim 42 is patentable over the cited art.

III.   Rejection of Claims 2 and 3 under 35 U.S.C. § 103(a)

Claims 2 and 3 were rejected under 35 U.S.C. 103(a) as being unpatentable over the '595 patent in view of U.S. Patent No. 5,596,569 (the '569 patent).

Claims 2 and 3 each ultimately depend from claim 1. As set forth with respect to claim 1, the '595 patent fails to disclose each limitation of claim 1. Applicants further assert that the '595 patent fails to teach or suggest each limitation of claim 1. The '569 patent in no way is asserted to affect the patentability of independent claim 1. Therefore, Applicants assert that claim 1 is patentable under 35 U.S.C. § 103(a) over the '595 patent in view of the '569 patent. Claims 2 and 3 each ultimately depend from claim 1 and therefore, should be patentable for at least the same reasons.

IV.   Rejection of Claim 5 under 35 U.S.C. §103(a)

Claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over *the '595 patent* in view of U.S. Publication No. 2001/00200254 (the '254 publication).

Claim 5 depends from claim 1. As set forth with respect to claim 1, the '595 patent fails to disclose each limitation of claim 1. Applicants further assert that the '595 patent fails to teach or suggest each limitation of claim 1. The '254 publication in no way is asserted to affect the patentability of independent claim 1. Therefore, Applicants assert that claim 1 is patentable under 35 U.S.C. § 103(a) over the '595 patent in view of the '254 publication. Claim 5 depends from claim 1 and therefore, should be patentable for at least the same reasons.

V.   Rejection of Claim 6 under 35 U.S.C. § 103(a)

Claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over the '595 patent in view of U.S. Patent No. 6,831,916 (the '916 patent).

Claim 6 depends from claim 1. As set forth with respect to claim 1, the '595 patent fails to disclose each limitation of claim 1. Applicants further assert that the '595 patent fails to teach or

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suggest each limitation of claim 1. The '916 patent in no way is asserted to affect the patentability of independent claim 1. Therefore, Applicants assert that claim 1 is patentable under 35 U.S.C. § 103(a) over the '595 patent in view of the '916 patent. Claim 6 depends from claim 1 and therefore, should be patentable for at least the same reasons.

VI.   Rejection of claims 7, 9-14, 16-18, 24-29, 32-34, 38, and 43-44 under 35 U.S.C. § 102(e)

Claims 7, 9-14, 16-18, 24-29, 32-34, 38, and 42-43 were rejected under 35 U.S.C. 103(a) as being unpatentable over the '595 patent in view of U.S. Patent No. 6,260,120 (the '120 patent). Because the '595 patent and the '120 patent, either alone or in combination, fail to teach or suggest each of the limitations of claims 7, 9-14, 16-18, 24-29, 32-34, 38, and 42-43, Applicants assert that these claims are patentable over the cited art.

Claims 7 and 9-14

Claims 7 and 9-14 each ultimately depend from claim 1. As set forth with respect to claim 1, the '595 patent fails to disclose each limitation of claim 1. Applicants further assert that the '595 patent fails to teach or suggest each limitation of claim 1. The '120 patent in no way is asserted to affect the patentability of independent claim 1. Therefore, Applicants assert that claim 1 is patentable under 35 U.S.C. § 103(a) over the '595 patent in view of the '120 patent. Claims 7 and 9-14 each ultimately depend from claim 1 and therefore, should be patentable for at least the same reasons.

Claims 16-18

Claims 16-18 each ultimately depend from claim 15. As set forth with respect to claim 15, the '595 patent fails to disclose each limitation of claim 15. Applicants further assert that the '595 patent fails to teach or suggest each limitation of claim 15. The '120 patent in no way is asserted to affect the patentability of independent claim 15. Therefore, Applicants assert that claim 15 is patentable under 35 U.S.C. § 103(a) over the '595 patent in view of the '120 patent. Claims 16-18 each ultimately depend from claim 15 and therefore, should be patentable for at least the same reasons.

<u>Claims 24-29 and 32-34</u>

Claim 24 recites:

> A storage network, comprising:
>   a switch including a plurality of linecards, each linecard including:
>   a plurality of ports, and
>   a plurality of <u>storage protocol processing units</u>, wherein each processing unit is associated with at least one port and <u>performs storage command processing</u> for commands received at said at least one port; and
>   a plurality of initiators and targets,
>   wherein a first set of initiators and targets operate in accordance with a first protocol and a second set of initiators and targets operate in accordance with a second protocol, and
>   wherein a third set of initiators and targets are local with respect to the switch and a fourth set of initiators and targets are remote with respect to the switch.

As shown with respect to claim 1, the '595 patent fails to disclose "a plurality of storage protocol processing units" that perform "storage command processing," as recited in claim 24. The '120 patent similarly fails to disclose such "storage protocol processing units." For example, with respect to Figure 1, the '120 patent discloses the same structure of Figure 1 of the '595 patent that was discussed above with respect to claim1. For example, the '120 patent also teaches that the port adaptors receive and forward access requests while the storage adaptors determine "where the data to be accessed resides on the storage devices, and reads the data from the storage devices and writes the data to the cache memory, for access by the port adaptor." *The '120 patent, col., 8, ll. 48-65.*

Even if the '120 and '595 patents are combined, the resulting combination does not teach or suggest " a plurality of storage protocol processing units" that perform "storage command processing." There is nothing with either reference, or their combination, to suggest the addition of such functionality to the port and storage adaptors described therein.

Because the '595 patent and '120 patent, either alone or in combination, fail to teach or suggest each of the limitations of claim 24, Applicants assert that claim 24 is patentable over the cited art. Claims 25-29 and 32-34 each ultimately depend from claim 24 and therefore, should be patentable for at least the same reasons.

Claim 38

Claims 38 ultimately depends from claim 35. Thus, the rejection in this section appears to be a typographical error. Nevertheless, Applicants will address the patentability of claim 38 including any combination of the '883 publication asserted against claim 35, as well as the '595 patent and '120 patent cited herein. As set forth with respect to claim 35, the '883 publication fails to disclose each limitation of claim 35. Applicants further assert that the '883 publication fails to teach or suggest each limitation of claim 35. The '595 patent and '120 patent are not asserted to affect the patentability of independent claim 35. Therefore, Applicants assert that claim 35 is patentable under 35 U.S.C. § 103(a) over the '883 publication, the '595 patent, and the '120 patent in any combination. Claims 38 depends from claim 35 and therefore, should be patentable for at least the same reasons.

Claims 43-44

> A method for use by a device in a system for storing and accessing data, the method comprising:
> receiving a packet from an initiator destined for a virtual target and formatted in accordance with a first protocol;
> determining if the packet is a data or control packet;
> if a data packet, sending the packet to a physical target formatted in accordance with a second protocol; and
> wherein all of the above steps are performed without buffering. *Emphasis added.*

The method of claim 43 recites that all of the steps are "performed without buffering." Alone or in combination, the '595 patent and '120 patent fail to teach or suggest the performance of these steps without buffering.

As shown above with respect to claim 21, the '595 patent fails to disclose "wire speed processing of packets." Likewise, the '595 patent fails to disclose, for example, "sending the packet to a physical target formatted in accordance with a second protocol," wherein this sending is "performed without buffering," as recited in claim 43. The '595 patent discloses a "cached storage subsystem." *See the '595 patent at Figure 1.* For example, the '595 patent teaches that one of its storage adaptors reads "the data from the storage devices and writes the data to the cache memory, for access by the port adaptor." *The '595 patent, col. 4, ll. 45-54.* Such a caching technique clearly

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entails buffering data or data packets. Accordingly, the '595 patent fails to disclose the performance of the recited steps "without buffering," as recited in claim 43. The '120 patent contains these exact same teachings of the '595 patent at col. 8, ll. 56-65, and thus, also fails to disclose the performance of these steps "without buffering."

Even if the '595 patent and '120 are combined, the resulting combination fails to teach or suggest the performance of steps such as "sending the data packet to a physical target formatted in accordance with a second protocol," where the step of sending is performed "without buffering." Both patents are directed specifically to a "cached storage subsystem" that utilizes a "cache memory 32" for buffering data transmitted between port and storage adaptors. Nothing within either reference or their combination, suggests a modification to the disclosed system that would facilitate unbuffered processing as recited in claim 43.

Because the '595 patent and the '120 patent, either alone or in combination, fail to teach or suggest each of the limitations of claim 43, Applicants assert that claim 43 is patentable over the cited art. Claim 44 depends from claim 43 and therefore, should be patentable for at least the same reasons.

VII. Rejection of Claims 30 and 31 under 35 U.S.C. § 103(a)

Claims 30 and 31 were rejected under 35 U.S.C. 103(a) as being unpatentable over the '595 patent in view of the '120 patent, further in view of the '569 patent.

Claims 30 and 31 each ultimately depend from claim 24. As set forth with respect to claim 24, the '595 patent in combination with the '120 patent fails to teach or suggest each limitation of claim 24. The '569 patent in no way is asserted to affect the patentability of independent claim 24. Therefore, Applicants assert that claim 24 is patentable under 35 U.S.C. § 103(a) over the '595 patent in view of the '120 patent, further in view of the '569 patent. Claims 30 and 31 each ultimately depend from claim 24 and therefore, should be patentable for at least the same reasons.

VIII. Rejection of Claims 19 and 22 under 35 U.S.C. § 103(a)

Claims 19 and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over the '595 patent in view of the '883 publication.

Claim 19 depends from claim 15 and claim 22 depends from claim 21. As set forth above, the '595 patent fails to disclose each limitation of claim 15 and claim 21. Applicants further assert that the '595 patent fails to teach or suggest each limitation of claim 15 and claim 21. The '883 publication in no way is asserted to affect the patentability of independent claims 15 and 21. Therefore, Applicants assert that claims 15 and 22 are patentable under 35 U.S.C. § 103(a) over the '595 patent in view of the '883 publication. Claims 19 and 22 each ultimately depend from claim 15 and claim 21, respectively, and therefore, should be patentable for at least the same reasons.

IX.   Rejection of Claim 23 under 35 U.S.C. § 103(a)

Claim 23 was rejected under 35 U.S.C. 103(a) as being unpatentable over the '595 patent in view of the '883 publication, further in view of the '120 patent.

Claim 23 ultimately depends from claim 21. As set forth with respect to claim 21, the '595 patent fails to disclose each limitation of claim 21. Applicants further assert that the '595 patent fails to teach or suggest each limitation of claim 21. Applicants further assert that the '883 publication fails to teach or suggest each limitation of claim 21, alone or in combination with the '595 patent. The '120 patent in no way is asserted to affect the patentability of independent claim 21. Therefore, Applicants assert that claim 21 is patentable under 35 U.S.C. § 103(a) over the '595 patent in view of the '883 publication, further in view of the '120 patent. Claim 23 depends from claim 21 and therefore, should be patentable for at least the same reasons.

X.   Rejection of claim 36 under 35 U.S.C. § 103(a)

Claim 36 was rejected under 35 U.S.C. 103(a) as being unpatentable over the '883 publication, further in view of the '595 patent.

Claim 36 depends from claim 35. As set forth with respect to claim 35, the '883 publication fails to disclose each limitation of claim 35. Applicants further assert that the '883 publication fails to teach or suggest each limitation of claim 35. The '595 patent in no way is asserted to affect the patentability of independent claim 35. Therefore, Applicants assert that claim 35 is patentable under 35 U.S.C. § 103(a) over the '883 publication in view of the '595 patent. Claims 36 depends from claim 35 and therefore, should be patentable for at least the same reasons.

XI.   Rejection of Claims 37 and 39 under 35 U.S.C. § 103(a)

Claims 37 and 39 were rejected under 35 U.S.C. 103(a) as being unpatentable over the '883 publication in view of the '120 patent.

Claims 37 and 39 each ultimately depend from claim 35. As set forth with respect to claim 35, the '883 publication fails to disclose each limitation of claim 35. Applicants further assert that the '883 publication fails to teach or suggest each limitation of claim 35. The '120 patent in no way is asserted to affect the patentability of independent claim 35. Therefore, Applicants assert that claim 35 is patentable under 35 U.S.C. § 103(a) over the '883 publication in view of the '120 patent. Claims 37 and 39 each ultimately depend from claim 35 and therefore, should be patentable for at least the same reasons.

XII.   Objection to Claim 9

Claim 9 was objected to for failing to have an end period. Appropriate correction has been made and withdrawal of the objection is respectfully requested.

XIII.   Conclusion

Based on the above amendments and these remarks, reconsideration of Claims 1-44 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.
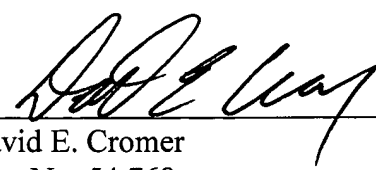
Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including today, October 13, 2005.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: __October 13, 2005__   By: _____

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